In the Claims

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1. (currently amended) Apparatus for providing efficient context switching between software tasks in ~~a manifold~~ an array ~~(ManArray)~~ one-by-one processor environment comprising:

a first set of registers stored in a first register file;

a second set of registers stored in a second register file;

a sequence processor/processing element (SP/PE) selection bit in an instruction; and

a context select bit (CSB) in a processor state register selecting a context of a first software task or a context of a second software task which in conjunction with the SP/PE selection bit determines which set of registers is to be accessed by the instruction.

2. (original) The apparatus of claim 1 in which the first register file is a sequence processor register file and the second register file is a processing element register file.

3. (original) The apparatus of claim 1 further comprising means for allowing the first set of registers to be saved and restored from memory in the background while a task is using the second set of registers in the foreground; and for allowing the second set of registers to be saved and restored from memory in the background while a task is using the first set of registers in the foreground.

4. (original) The apparatus of claim 3 wherein said means for allowing comprises a pair of background address registers to provide store and load addresses.

5. (original) The apparatus of claim 1 further comprising a plurality of execution units and a multiplexer connected to select which registers the execution units read data from and write data to, the multiplexer controlled by a logical combination of the SP/PE selection bit and the CSB.

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6. (currently amended) The apparatus of claim 1 wherein the SP/PE selection bit is used in a 1x1 array core having SP register files and PE register files to determine whether ~~which register files~~ the SP's register files or the PE's registers files are to be accessed for each instruction execution when the CSB is inactive and to have both SP and PE instructions use the PE register files when the CSB is active.

7. (original) The apparatus of claim 1 wherein the first or second register files may comprise reconfigurable compute register files (CRF), address register files (ARF), miscellaneous register files (MRF) or a combination of CRF, ARF and MRF files.

8. (currently amended) Apparatus for providing efficient context switching between tasks in ~~a manifold~~ an array ~~(ManArray)~~ of multiple processors ~~environment in which~~ including a sequence processor (SP) and multiple processing elements (PE) ~~are employed~~, said apparatus comprising:

a first set of registers stored in a first register file for the SP;

~~a second set~~ additional sets of registers stored in ~~a second~~ additional register file files, with one of the additional sets of registers for each of the PEs;

a sequence processor/processing element (SP/PE) selection bit in an instruction; and

a software controllable context select bit (CSB) in a processor state register which in a logical combination with the SP/PE selection bit reconfigures the array ~~ManArray~~ by selecting a first context in which the array ~~ManArray~~ is configured in a first configuration or a second context in which the array ~~ManArray~~ is configured in a second configuration.

9. (currently amended) The apparatus of claim 8 wherein said array ~~ManArray~~ is a 1x2 array and said first configuration is a 1x2 and said second configuration is a 1x1.

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10. (currently amended) The apparatus of claim 8 wherein said array ~~ManArray~~ is a 1x5 array and said first configuration is a 1x5 and said second configuration is a 2x2.

11. (currently amended) A method for providing efficient context switching in a ~~manifold~~ array processor having a sequence processor and multiple processing elements, the method comprising:

setting a sequence processor/processing element (SP/PE) selection bit in an instruction;

setting a context select bit (CSB) in a processor state register;

utilizing the SP/PE selection bit in conjunction with the context select bit to determine a context for operation; and

configuring the manifold array processing depending upon the context.

12. (currently amended) The method of claim 11 further comprising the steps of:

identifying each PE of said ~~manifold~~ array with both a virtual identifier and a physical identifier; and

identifying each PE utilizing its physical identifier in a first context and identifying each PE utilizing its virtual identifier in a second context.

13. (original) The method of claim 12 wherein the first context is when the CSB bit is inactive and the second context is when the CSB bit is active.